

# Hash-Based Signatures



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Supported by DFG and DAAD

## Part XI: XMSS in Practice

# Hash functions & Blockciphers



AES

Blowfish

3DES

Twofish

Threefish

Serpent

IDEA

RC5

RC6

...

SHA-2

SHA-3

BLAKE

Grøstl

JH

Keccak

Skein

VSH

MCH

MSCQ

SWIFFTX

RFSB

...

# PRF and Hash Function from AES



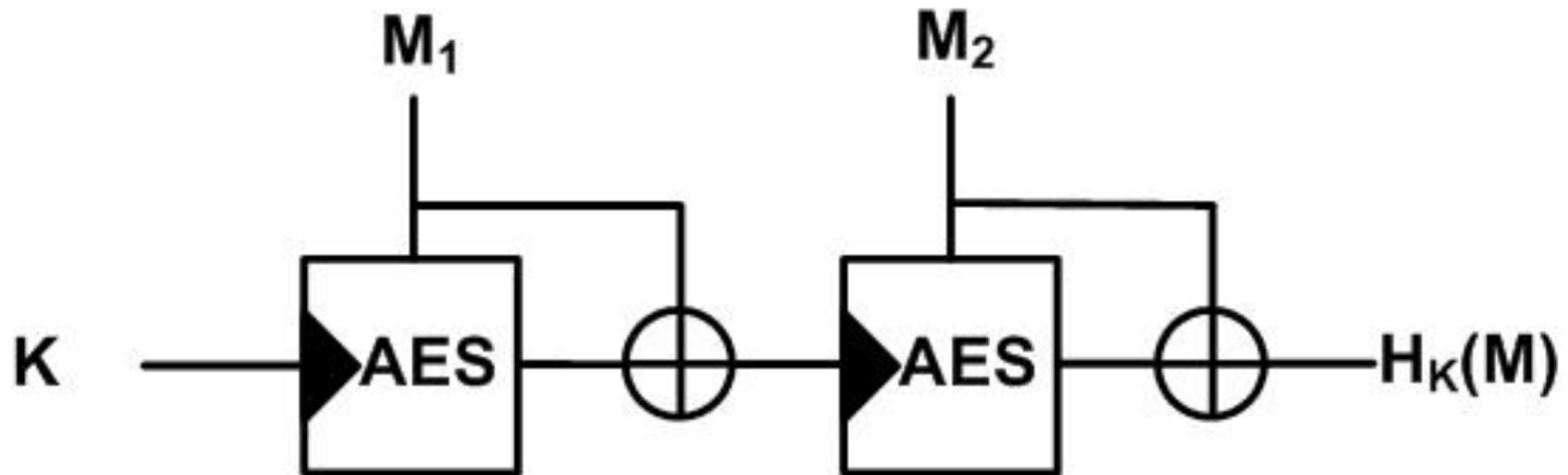
AES:  $\{0,1\}^{128} \times \{0,1\}^{128} \rightarrow \{0,1\}^{128}$

## PRF:

- Plain AES

## Hash function

- AES with Matyas-Meyer-Oseas in Merkle-Damgård mode



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# PRF and Hash Function from SHA2



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**SHA2:**  $\{0,1\}^* \rightarrow \{0,1\}^{256}$

## PRF

- Simplified **SHA2-HMAC**:

$$F_K(M) = \text{SHA2}(\text{Pad}(K) \parallel M)$$

- $\text{Pad}(x)$  prepends 0's to reach blocksize (512bit)
- No MD-Strengthening needed

## Hash function

- Plain SHA2
-

# XMSS Implementations

## C Implementation



C Implementation, using OpenSSL [BDH2011]

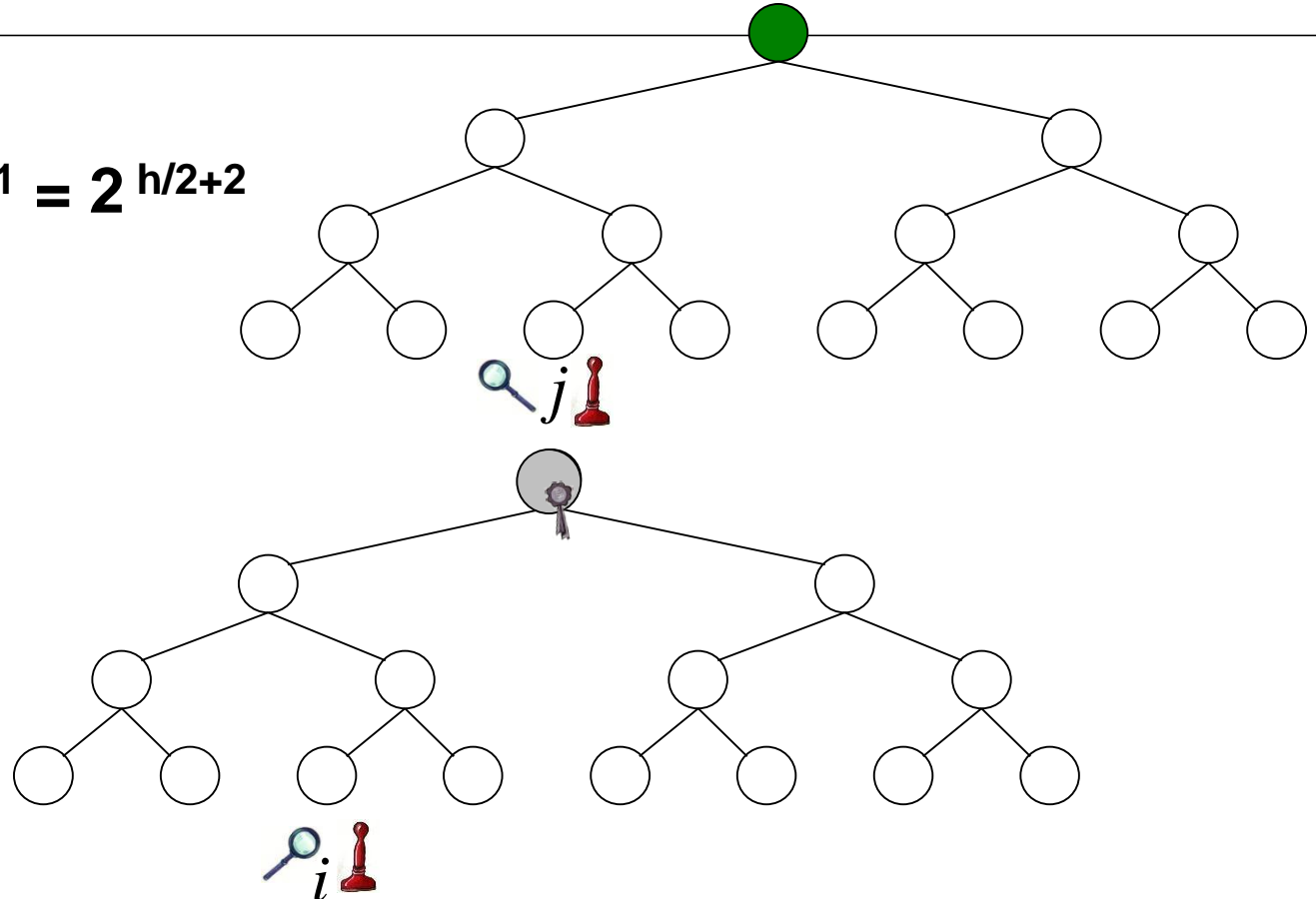
	Sign (ms)	Verify (ms)	Signature (bit)	Public Key (bit)	Secret Key (byte)	Bit Security	Comment
XMSS-SHA-2	35.60	1.98	<b>16,672</b>	13,600	3,364	157	h = 20, w = 64,
XMSS-AES-NI	<b>0.52</b>	<b>0.07</b>	19,616	7,328	1,684	84	h = 20, w = 4
XMSS-AES	1.06	0.11	19,616	7,328	1,684	84	h = 20, w = 4
RSA 2048	<b>3.08</b>	<b>0.09</b>	≤ 2,048	≤ 4,096	≤ 512	87	

Intel(R) Core(TM) i5-2520M CPU @ 2.50GHz with Intel AES-NI

# Reminder: Tree Chaining



$$2^{h+1} \rightarrow 2 * 2^{h/2+1} = 2^{h/2+2}$$



**But: Larger signatures!**

# XMSS Implementations

## Smartcard Implementation



	Sign (ms)	Verify (ms)	Keygen (ms)	Signature (byte)	Public Key (byte)	Secret Key (byte)	Bit Sec.	Comment
XMSS	<b>134</b>	23	<b>925,400</b>	2,388	800	2,448	92	H = 16, w = 4
XMSS+	<b>106</b>	25	<b>5,600</b>	3,476	544	3,760	94	H = 16, w = 4
RSA 2048	190	7	11,000	≤ 256	≤ 512	≤ 512	87	

Infineon SLE78 16Bit-CPU@33MHz, 8KB RAM, TRNG, sym. & asym. co-processor

NVM: Card 16.5 million write cycles/ sector,  
XMSS+ < 5 million write cycles (h=20)

[HBB12]

**Thank you!**  
**Questions?**

